Docket No.: W&B-INF-1960

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ROBERT KAISER ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR COMPARING THE ADDRESS OF A MEMORY ACCESS WITH AN ALREADY KNOWN ADDRESS OF A FAULTY MEMORY CELL

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

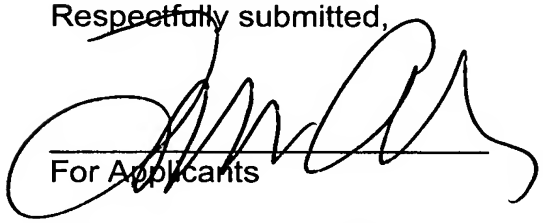
In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,115,828 (Tsutsumi et al.), dated September 5, 2000;

Lucente, M. A. et al.: "Memory System Reliability Improvement Through Associative Cache Redundancy", IEEE Journal of Solid State Circuits, Vol. 26, No. 3, March 1991, pages 404–409;

International Search Report, dated August 11, 2003.

Respectfully submitted,



For Applicants

LAURENCE A. GREENBERG
REG. NO. 29,308

LAURENCE A. GREENBERG
REG. NO. 29,308

Date: October 20, 2003
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101
/nt/kf

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: W&B-INF-1960 Appl. No.: Applicant: ROBERT KAISER ET AL. Filing Date: October 20, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,115,828	9/5/00	Tsutsumi et al.			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Lucente, M. A. et al.: "Memory System Reliability Improvement Through Associative Cache Redundancy", IEEE Journal of Solid State Circuits, Vol. 26, No. 3, March 1991, pages 404–409

EXAMINER	DATE CONSIDERED